REMARKS/ARGUMENTS

Claims 27-52 are pending in the application. Claims 27, 38, 49, and 51 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

MISSING REFERENCE

In the office action dated 09/24/04, the Examiner first relied on U.S. Patent No. 4,862,452 (Milton et al.) to reject claims. However, that reference was not listed on the PTO-892 Form that accompanied that office action. The Milton reference does not appear to have been formally acknowledged by the Examiner.

In the amendment filed in response to the previous office action dated 06/06/05, the Applicant requested that the Examiner list the Milton reference on a PTO-892 Form in order to formally acknowledge that reference. The Examiner included a PTO-892 Form with the pending final office action dated 11/28/05, in order to cite the Schwarz reference, but the Examiner again failed to formally acknowledge the Milton reference.

The Applicant hereby repeats the previous request that the Examiner list the Milton reference on a PTO-892 Form in order to formally acknowledge that reference.

Prior-Art Rejections

In paragraph 3 of the final office action, the Examiner rejected claims 27-52 under 35 U.S.C. 103(a) as being unpatentable over Milton in view of Schwarz. For the following reasons, the Applicant submits that all of the pending claims are allowable.

Claims 27, 38, 49, and 51

Claim 27 has been amended to recite that the data signal has two or more data bits, where the signal unit analyzes the bit value of each of two or more data bits in the data signal. Support for these amendments to claim 27 is found in previously presented claim 28, which depends from claim 27 and which recites that "the data signal has a plurality of analyzed data bits having the specified value." The Applicant submits that the only way for the data signal of claim 28 to have a plurality of analyzed data bits is for the data signal to have two or more data bits, where the signal unit analyzes the bit value of each of two or more data bits in the data signal. Since the amendments to claim 27 simply recite features that are inherent to the recitations in previously pending claim 28, the Applicant submits that the amendments to claim 27 do not raise any new issues. The same is true for claim 38, 49, and 51. The Applicant submits therefore that it would be improper to refuse to enter the current amendment.

As a result of the current amendment, currently amended claim 27 is directed to a method for applying one or more interrupt signals in a system comprising a first processor and one or more other processors. According to claim 27, a first processor generates a data signal having two or more data bits, wherein each data bit has either a first bit value or a second bit value. The data signal is transmitted from a data port of the first processor to a signal unit external to the first processor and the one or more other processors. The signal unit converts the data signal into one or more interrupt signals by analyzing the bit value of each of two or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal. Each interrupt signal is transmitted from the signal unit to an interrupt port of an other processor.

In the non-limiting example of Fig. 2:

- o DSP0 22 is an example of the first processor of claim 27;
- o Signal unit 23 is an example of the signal unit of claim 27; and
- o DSP1 24 is an example of one of the one or more other processors of claim 27.

In this exemplary embodiment, DSP0 generates and transmits the multi-bit data signal of claim 27 to signal unit 23 via shared data bus 26. Signal unit 23 converts the data signal from DSP0 into one or more interrupt signals by analyzing the bit value of each of two or more data bits in the multi-bit data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal. Signal unit 23 transmits each interrupt signal, e.g., to an interrupt port of DSP1 or another DSP (e.g., via one of dedicated interrupt lines SIGNAL1-SIGNAL8 or another dedicated interrupt line to another DSP).

In rejecting claim 27, the Examiner cited Milton as teaching examples of the first processor, the signal unit, and the one or more other processors of claim 27. In particular, on page 2, the Examiner refers to "DSP module" as an example of the first processor of claim 27 and "plurality of DSP modules" as examples of the one or more other processors of claim 27, and, on page 3, the Examiner cites column 2, lines 43-53, as teaching an example of the signal unit of claim 27.

Based on these passages in the final office action, the Applicant assumes that the Examiner believes that:

- o One of DSP modules 13 in Fig. 1 of Milton is an example of the first processor of claim 27;
- o The other two DSP modules 13 in Milton's Fig. 1 are examples of the one or more other processors of claim 27; and
- o Main controller 1 in Milton's Fig. 1 is an example of the signal unit of claim 27.

The Applicant requests clarification if any of these assumptions are incorrect.

According to Milton, main controller 1 and DSP modules 13 communicate using an interrupt handshaking scheme in which a predetermined DSP module 13 generates a TMSINT 5 interrupt control signal for application to the interrupt input INT of main controller 1. See column 2, lines 60-66. In response, among other actions, main controller 1 generates an appropriate clear interrupt signal via a CLRINT output thereof for causing the selected DSP module 13 to reset its TMSINT 5 signal output. See column 3, lines 4-7.

Thus, according to the express teachings in Milton, a particular DSP module 13 transmits an interrupt control signal (TMSINT 5) to main controller 1, and main controller 1 responds by transmitting a clear interrupt signal (CLRINT) to that very same DSP module 13. Thus, even if interrupt control signal TMSINT 5 were interpreted to be an example of the data signal of claim 27 (which, for the reasons given below, the Applicant does not admit), the clear interrupt signal CLRINT cannot be an example of the one or more interrupt signals of claim 27, because the clear interrupt signal CLRINT is not transmitted from main controller 1 to "an other processor," as explicitly recited in claim 27. Rather, the clear interrupt signal CLRINT is transmitted from main controller 1 back to the very same DSP module 13 that transmitted the original interrupt control signal TMSINT 5 to the main controller.

As suggested above, the Applicant submits further that interrupt control signal TMSINT 5 is not an example of the data signal of claim 27. Milton explicitly teaches that interrupt control signal

TMSINT 5 is a tristate signal. See column 7, lines 1-2. As known to those skilled in the art, a tristate signal is an analog signal having one of three different states: a high-level state, a low-level state, or a high-impedance, floating-level state. A tristate signal is not "a data signal having two or more data bits," as explicitly recited in claim 27.

Moreover, according to claim 27, the signal unit converts the data signal into one or more interrupt signals by analyzing the bit value of each of two or more data bits, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal. Milton's main controller 1 does not analyze "the bit value of each of two or more data bits" in a data signal, because interrupt control signal TMSINT 5 does not have two or more data bits.

In the invention of claim 27, if two or more data bits in the data signal have the specified bit value, then the signal unit will generate two or more different interrupt signals. Milton contains no such teachings. In Milton, each interrupt control signal TMSINT 5 results in the generation of a single clear interrupt signal CLRINT. There is no teaching or even suggestion in Milton that a single interrupt control signal TMSINT 5 results in the generation of two or more different clear interrupt signals CLRINT.

In view of the foregoing, the Applicant submits that the Examiner mischaracterized the teachings in Milton or misinterpreted the recitations of claim 27 or both in rejecting claim 27. In fact, the Applicant submits that Milton does not teach a first processor that generates and transmits a data signal having two or more data bits to a signal unit that converts the data signal into one or more interrupt signals by analyzing the bit value of each of two or more data bits in the data signal, wherein each analyzed data bit in the data signal having a specified bit value corresponds to a different interrupt signal, and wherein the signal unit transmits each interrupt signal to an interrupt port of an other processor.

Nor does Schwarz provide the features of claim 27 missing from Milton.

For all these reasons, the Applicant submits that claim 27 is allowable over the cited references. For similar reasons, the Applicant submits that claims 38, 49, and 51 are allowable over the cited references. Since the rest of the claims depend variously from claims 27, 38, 49, and 51, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under Section 103(a) have been overcome.

Claims 28, 39, and 52

According to claim 28, the data signal has a plurality of analyzed data bits having the specified value, the signal unit converts the data signal into a plurality of interrupt signals, and each interrupt signal is transmitted to a different interrupt port of an other processor.

With regard to claim 27, the Applicant argued in the previous section that, if two or more data bits in the data signal have the specified bit value, then the signal unit will generate two or more different interrupt signals. Claim 28 explicitly recites these inherent features of claim 27.

The Applicant submits that this provides further reason for the allowability of claim 28 as well as claims 39 and 52 over the cited references.

Claims 29, 40, and 52

According to claims 29, 40, and 52, at least two interrupt signals are transmitted to two different interrupt ports of a single other processor. In rejecting claim 29, the Examiner stated that Milton teaches this feature, citing column 2, lines 21-63, and column 1, lines 58-68. The Applicant submits that, in fact, Milton does not teach, either in the cited passages or anywhere else, that at least two interrupt signals are transmitted to two different interrupt ports of a single other processor. In particular, each DSP module 13 in Milton's Fig. 1 is depicted with a single interrupt port connected to receive a single interrupt clear signal from main controller 1.

The Applicant made these exact same remarks in response to the previous rejection of claims 29, 40, and 52 by the Examiner. The Examiner completely ignored the Applicant's remarks and simply restated the previous rejection verbatim with no further explanation and no explicit citation of exactly which single DSP module 13 in Milton receives at least two interrupt signals at two different ports.

The Applicant submits that this provides additional reasons for the allowability of claims 29, 40, and 52 over the cited references.

Claims 33 and 44

According to claims 33 and 44, the first processor transmits an address signal to the signal unit, where the signal unit compares the address signal to a specified value to determine whether to store the two sequential values in the two registers. In rejecting claim 33, the Examiner stated that Milton teaches this feature, citing column 1, lines 58-68, and column 4, lines 44-55. The Applicant submits that, in fact, Milton does not teach, either in the cited passages or anywhere else, that a first processor transmits an address signal to a signal unit that compares the address signal to a specified value to determine whether to store the two sequential values in the two registers. In particular, neither column 1, lines 58-68, nor column 4, lines 44-55, teaches anything about a signal unit comparing an address signal to a specified value to determine whether to store two sequential values of a data signal in two registers.

The Applicant made these exact same remarks in response to the previous rejection of claims 33 and 44 by the Examiner. Here, too, the Examiner completely ignored the Applicant's remarks and simply restated the previous rejection verbatim with no further explanation and no explicit citation of exactly which DSP module 13 in Milton transmits an address signal to main controller 1.

The Applicant submits that this provides additional reasons for the allowability of claims 33 and 44 over the cited references.

Claims 35, 46, 50, and 52

According to claim 35, the data signal is transmitted from the first processor to the signal unit via a shared data bus. In rejecting claim 35, the Examiner cited Milton's "bidirectional PCM links" as an example of the shared data bus of claim 35. As far as the Applicant can determine, the most relevant bidirectional PCM links taught in Milton are those between circuit switch matrix 3 and the various DSP modules 13. Significantly, however, even assuming that interrupt control signal TMSINT 5 is "the data signal" of claim 35 (which the Applicant does not admit), the fact remains that interrupt control signal TMSINT 5 is not transmitted from any DSP module 13 to main controller 1 via any of bidirectional PCM links 15. Just because Milton teaches a data bus somewhere in its specification, that does not mean that the Examiner is free to replace a completely different signal line in Milton's system with such a data bus without any suggestion in the art for doing so. The Applicant submits that there is no suggestion or

motivation in the prior art for transmitting a tristate interrupt signal, such as TMSINT 5, over a shared data bus, such as a bidirectional PCM link.

The Applicant submits that this provides additional reasons for the allowability of claim 35 and also claims 46, 50, and 52 over the cited references.

Claims 36 and 47

Claims 36 and 47 recite an "other signal unit" (i.e., different from the "signal unit" previously recited in claims 27 and 38). In rejecting claim 36, the Examiner stated that Milton teaches the features recited in that claim, stating that "Milton teaches switching and bidirectional communication of DSP modules as well as Circuit switch matrix 3 and a Peripheral Switch Matrix 5D." The Applicant submits that, just because Milton might teach "switching and bidirectional communication of DSP modules" (which the Applicant does not necessarily admit), that does not mean that Milton teaches two different signal units operating in conjunction with those DSP modules.

According to the Examiner, DSP modules 13 of Milton's Fig. 1 are examples of the first processor and one or more other processors of claim 27. Although the Examiner does not explicitly say so, presumably, the Examiner believes that Milton's main controller 1 is an example of the signal unit of claim 27. Significantly, Milton does not teach more than just that one main controller receiving and transmitting interrupt signals from and to the DSP modules. As such, Milton does not teach or even suggest an example of the "other signal unit" recited in claims 36 and 47.

The Applicant submits that this provides additional reasons for the allowability of claims 36 and 47 (and therefore claims 37 and 48) over the cited references.

In view of the above amendments and remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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